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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,651	12/29/2000	Robert C. Glenn	42390P9716	1502

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EXAMINER	
LAMARRE, GUY J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,651	GLENN ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006 and 27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/27/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL OFFICE ACTION

1. This office action is in response to Applicants' Amendment of 09 January 2006.

1.1 **Claims** 1 and **3-24** remain pending.

1.2 The prior art rejections of record to **the Claims** are maintained in response to Applicants' **Amendment**.

Response to Arguments

2. Applicants' arguments of 09 January 2006 have been fully considered, but they are not persuasive.

REMARKS

3. **Examiner** notes that the reference by **Nelson et al.** is (USPN **5467040)** contrary to what is reflected in Applicants' response at page 2 para. 2.

3.0 In response to **Claims** 1 **and** 3-24, Applicants allege that the prior art of record is "silent as to the location of skew measurement, as to implementation in plural semiconductor chips"

Examiner disagrees as it cannot be understood how Applicants fail to realize that skew can be compensated for only after measuring such skew or skew cannot be compensated for if not measured at a destination/receiving side.

Examiner further disagrees as the prior art of record, e.g., **Nelson et al.**, col. 2 line 7 – col. 3 line 42, clearly discloses measuring a skew at a destination or end of line and compensating for such skew via plural adjusting/insertion techniques at the transmit end.

Nelson et al. clearly discloses that use of plural semiconductor chips may be required for implementing such skew measuring and implementing compensation therefor, e.g., at col. 3 line 36.

Therefore, the **Examiner** maintains that the prior art of record renders unpatentable **Claims 1, 8, 17** and the claims depending thereon, i.e., the prior art of record renders unpatentable **Claims 1** and **3-24.**

Claim Rejections - 35 USC ' 102

3.1 **Claims 1, 3-29** are rejected under 35 U.S.C. 102 (e) as being anticipated by **Widmer** (US Patent No. 6,496,540; Filed: July 22, 1998).

Widmer discloses, e.g., Fig. 6, skew adjustment algorithm in "Transformation of parallel interface into coded format with preservation of baud-rate" wherein

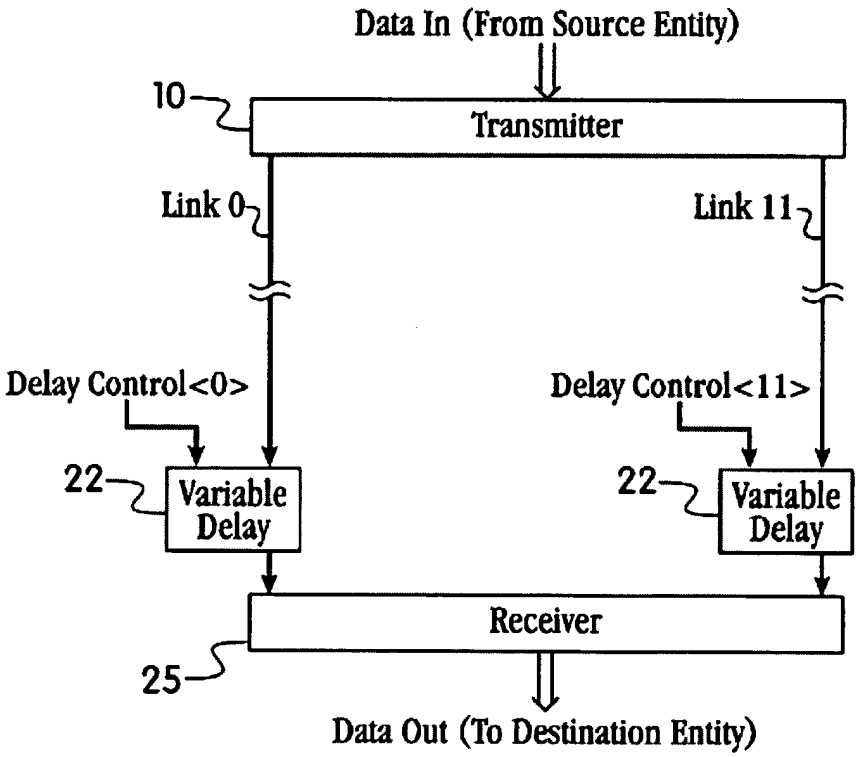


Fig. 6

"the step of adjusting transmission delay by a dynamically adjustable delay in each transmission link may be included. The step of retiming coded data blocks on each link with a dedicated adjustable clock, and the step of eliminating skew among the links by providing a second retiming of data transferred on the links at a rate less than the predetermined baud rate with a clock system shared by all links may be included. The steps of receiving transmitted coded data blocks from the transmission lines at a receiver end is preferably included. The step of checking disparity to determine errors in the data blocks at the receiver end may be included. The step of encoding may further include the steps of outputting data blocks from each encoder to a disparity register and inputting disparity data from each disparity register to the encoder associated the disparity register to create a running disparity check of the data blocks. Further steps may include such as deserializing the serially transmitted coded data blocks at a receiver end to provide parallel coded data blocks, decoding the data blocks at a deserialized rate, the deserialized rate being lower than the predetermined baud rate and multiplexing the decoded data blocks to provide parallel data blocks at the predetermined baud rate. Each uncoded data block may include 10 bits and the predetermined baud rate may be greater than or equal to about 2 Gbaud."

As per Claims 1, 3-29, Widmer depicts, e.g., in Fig. 6 and related description in col. 1 line 13 et seq., the claimed method, comprising: a) measuring a skew between a data signal and a clock signal at a receiving end of a serial link; and b) adjusting (col. 2 line 27) a phase relationship between said data signal (col. 2 line 30) and said clock signal (col. 2 line 29) to reduce said skew via variable delay means implementable in hardware or software, e.g., in CPU or other digital component: Refer, e.g., to Fig. 6: block 22 and col. 2 line 23 et seq.

Widmer teaches means wherein said adjusting of said phase relationship occurs at a transmitting end of said serial link in col. 9 line 46; further comprising receiving said measured skew at a skew adjustment unit and determining said phase relationship before said adjusting a

phase relationship in col. 2 line 27 and col. 10 line 23; further comprising programming said phase relationship into a semiconductor chip or IC chip in col. 9 line 27 and col. 11 line 15.

Widmer further teaches means wherein said adjusting a phase relationship further comprises imposing a delay on at least one of said signals in col. 2 line 27, e.g., "*Referring to FIG. 8, each of twelve deserializers 26 is controlled by clocks (CLK<0:11>) derived from the phase adjusted clock 20 for that particular link. After deserialization to a six-line/link width, data remains stable for intervals of close to 3 ns. Thus, if the skew between any two links remains well within these limits, there is enough margin to reclock all 72 lines of the twelve links at this point with a set of clocks CLKS<0:5> to eliminate the skew. The clocks CLKS<0:5> are 1/6th-rate clocks staggered by 0.5 ns but otherwise of uniform phase and all originating from a shared source clock, e.g. CLKS<0> which is aligned with the serial bit-stream of link#0. This common set of clocks controls all functions thereafter to the point where the data is placed into a storage cell of a buffer 30 through decoders 28 and a multiplexer 29. All functions at the output side of buffer 30 are usually controlled by a clock provided by a destination entity, as indicated in FIG. 8.*"

Widmer further teaches means to impose delay on one or both signals as seen in Fig. 6. And wherein said adjusting a phase relationship further comprises adjusting a phase offset between a pair of phasors associated with a pair of phase interpolators, a first of said phasors used to derive a second clock signal that times the transmission of said data signal, a second of said phasors used to derive said clock signal in col. 2 line 27 wherein equivalent means are provided for eliminating skews via multiple values of a period to effectively result in phase interpolation means. Also refer to Fig. 6 wherein variable delay blocks 22 are configured to delay signals on the links by more than 360 degrees.

Widmer further teaches that such skew adjustment approach may be used in data communications such as network interface corresponding to a physical layer or wherein said network interface corresponds to a media access control layer, or other transmission system where signals may require synchronization, e.g. col. 1 line 8.

3.2 Claims 1, 3-29 are rejected under 35 U.S.C. 102(b) as being anticipated by **Nelson et al.** (US Patent No. 5,467,040; 14 Nov.1995).

As per Claims 1, 3-29, Nelson et al. anticipates the claimed technique for adjusting clock skew comprising: means for measuring skew between a test/clock signal and a data signal at a destination of a link (Fig. 4 *numeral 44*), means for determining amount of skew compensation required, and means for injecting (Fig. 4 *block 26*) such amount of skew compensation into the sending side (Fig. 4 *numeral 34*) of such link, e.g., in Figs. 4 & 12 and related description at col. 1 line 8 et seq.

Nelson et al. discloses, in Figs. 1-12 and related description, '*an apparatus and method of compensating for skew (time difference) between electrical signals, and a system for generating and distributing skew-compensated signals. More particularly, the present invention relates to a skew compensation circuit capable of providing electronic adjustment in sub-nanosecond increments, methods of adjusting and initializing skew compensation circuits, a pulse generator using a skew compensation circuit to precisely adjust the width of the pulse, and a clock distribution system for providing skew compensated clock signals, suitable for use in a high speed computer system.*'

Nelson et al. anticipates the claimed invention since disclosed thereby is a method '*for adjusting signal delay on an electronic module having a clock input port, a test point, and a skew compensation circuit, including the steps of injecting a test signal into the clock port of the module; measuring signal delay between the clock port and the test point; comparing the measured signal delay to the desired signal delay; calculating the amount of adjustment needed to cause the measured signal delay*

to equal the desired signal delay; selecting a delay code that reflects the calculated amount of adjustment; and programming the skew compensation circuit according to the selected delay code.'

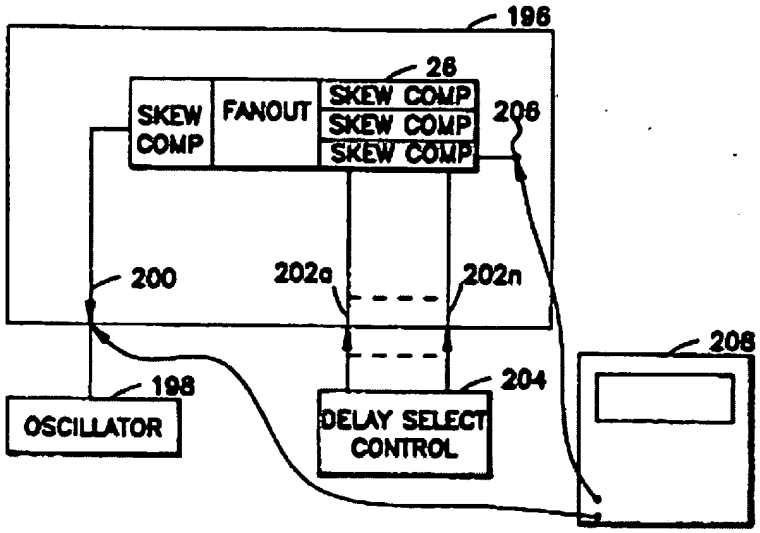


FIG. 12

Claim Rejections - 35 USC ' 103

4.1 **Claims 1, 3-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Widmer** (US Patent No. 6,496,540; Filed: July 22, 1998) and **Nelson et al.** (US Patent No. 5,467,040; 14 Nov.1995).

As per Claims 1, 3-29, Widmer substantially depicts, e.g., in Fig. 6 and related description in col. 1 line 13 et seq., the claimed method, comprising: a) measuring a skew between a data signal and a clock signal at an end of a serial link; and b) adjusting at end of the serial link (col. 2 line 27) a phase relationship between said data signal (col. 2 line 30) and said clock signal (col. 2 line 29) to reduce said skew via variable delay means implementable in hardware or software, e.g., in CPU or other digital component: Refer, e.g., to Fig. 6: block 22 and col. 2 line 23 et seq.

Not specifically described in detail by **Widmer** is the step whereby the end of the serial link is the receiving end or the skew compensation is effected at a transmit end or how such skew

compensation is caused.

However the point where skew is measured or the location of skew adjustment or the means used in effecting such skew adjustment is not restricted exclusively to a specific point of application by **Widmer.** Those of ordinary skill in memory testing and skew compensation will recognize that the ability to effect such timing is a circuit design choice.

Accordingly, Nelson et al., in an analogous art, discloses skew compensation wherein skew is detected at the receiving end of end of the serial link, such skew being compensated at the transmit end wherein such skew compensation is caused by adjusting phase of a signal. {See **Nelson et al.**, Id., e.g., Figs. 4 & 12 and col. 5 line 23 et seq.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the process of **Widmer** by including therein the sync techniques as disclosed by **Nelson et al.** because such modification would provide the procedure of **Widmer** with a method whereby '*the entire clock distribution can be adjusted to compensate for skew in the signals*,' or skew compensation can be performed at any convenient point in a link, thereby providing flexibility to the system operator." {See **Nelson et al.**, Id., col. 13 line 14 et seq.}

Conclusion

* **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

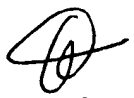
Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Guy J. Lamarre, P.E
Primary Examiner